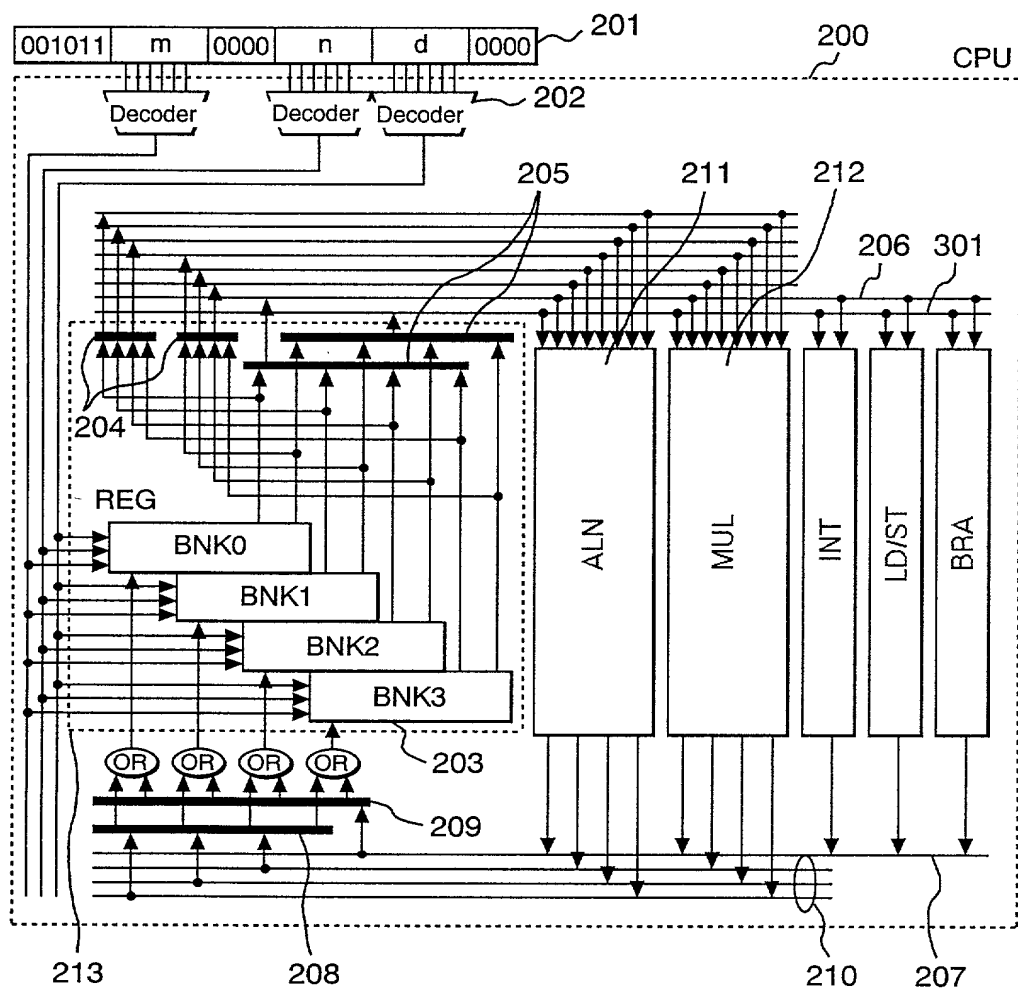
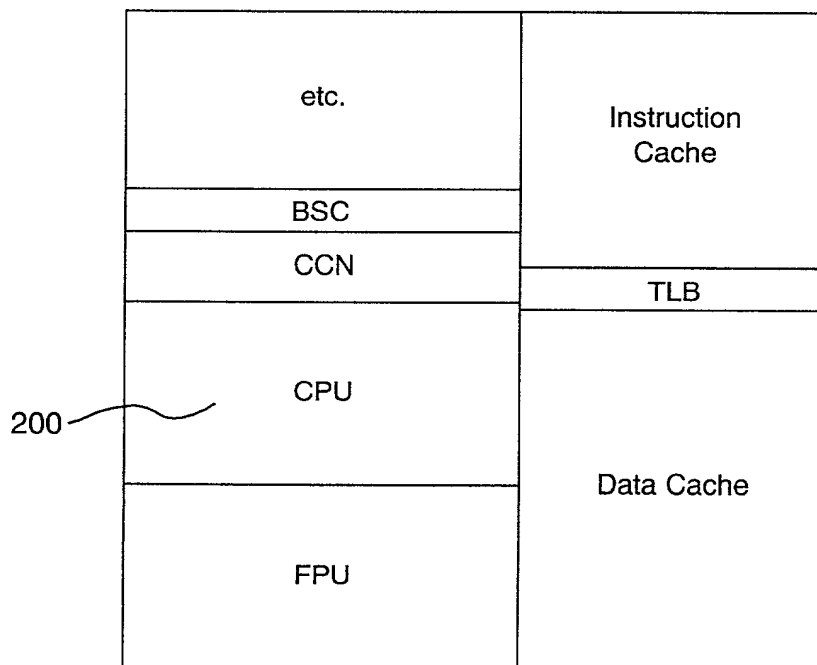


**FIG. 1**



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**FIG. 2**

**FIG. 3**

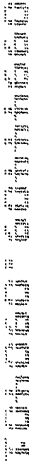


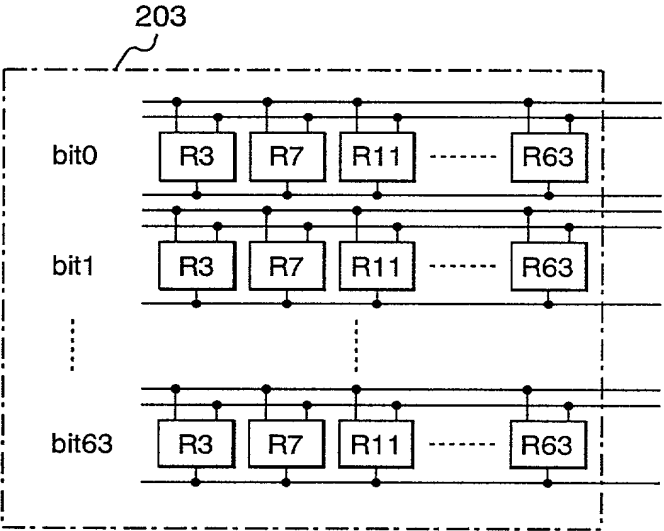
FIG. 4

a	b	c	d	e	f	R0	R1	R2	R3	R4	R5	R6	R7	R8		R59	R60	R61	R62	R63
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0		0	0	0	0	0
0	0	0	0	0	1	0	1	1	1	1	0	0	0	0		0	0	0	0	0
0	0	0	0	1	0	0	0	1	1	1	1	0	0	0		0	0	0	0	0
0	0	0	0	1	1	0	0	0	1	1	1	1	0	0	.....	0	0	0	0	0
0	0	0	1	0	0	0	0	0	1	1	1	1	1	0		0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	1	1	1	1		0	0	0	0	0
0	0	0	1	1	0	0	0	0	0	0	1	1	1	1		0	0	0	0	0
		...							...									...		
1	1	1	0	1	1	0	0	0	0	0	0	0	0	0		1	1	1	1	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0		0	1	1	1	1
1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	.....	0	0	1	1	1
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0		0	0	0	1	1
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0		0	0	0	0	1

FIG. 5

a	b	To 206		To 307		
0	0	X0		X1	X2	X3
0	1	X1		X2	X3	X0
1	0	X2		X3	X0	X1
1	1	X3		X0	X1	X2

FIG. 6



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**FIG. 7**

a	b	input			output			
0	0	X	Y	Z	0	X	Y	Z
0	1	X	Y	Z	Z	0	X	Y
1	0	X	Y	Z	Y	Z	0	X
1	1	X	Y	Z	X	Y	Z	0

**FIG. 8**

a	b	X	output			
0	0	X	X	0	0	0
0	1	X	0	X	0	0
1	0	X	0	0	X	0
1	1	X	0	0	0	X

FIG. 9

PACK.W Rm, Rn, Rd

xxxxxx	m	xxxxx	n	d	0000
31	26 25	20 19	16 15	10 9	4 3 0

operation

source [1] ← SignExtend<sub>64</sub>(Rm);

source [2] ← SignExtend<sub>64</sub>(Rm+1);

source [3] ← SignExtend<sub>64</sub>(Rm+2);

source [4] ← SignExtend<sub>64</sub>(Rm+3);

amount ← ZeroExtend<sub>64</sub>(Rn);

REPEAT i FROM 0 FOR 4

result [i] ← ZeroExtend<sub>16</sub>(source[i] >> amount);

Rd ← MultiRegister<sub>16</sub>(result);

FIG. 10

PACKI.W Rm, s, Rd

xxxxxx	m	s	d	0000
31	26 25	20 19	10 9	4 3 0

operation

source [1] ← SignExtend<sub>64</sub>(Rm);

source [2] ← SignExtend<sub>64</sub>(Rm+1);

source [3] ← SignExtend<sub>64</sub>(Rm+2);

source [4] ← SignExtend<sub>64</sub>(Rm+3);

amount ← SignExtend<sub>10</sub>(s);

REPEAT i FROM 0 FOR 4

result [i] ← ZeroExtend<sub>16</sub>(source[i] >> amount);

Rd ← MultiRegister<sub>16</sub>(result);

FIG. 11

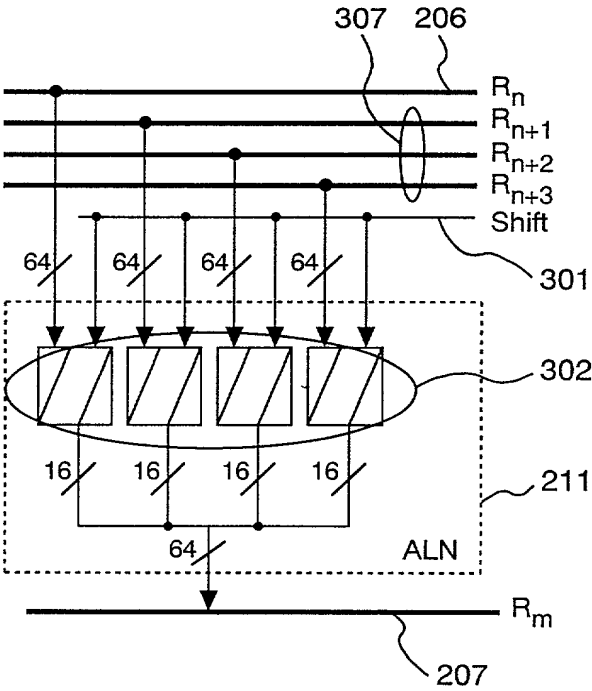


FIG. 12

UNPACK.W Rm, Rd

xxxxxx	m	xxxxx	000000	d	0000
31	26 25	20 19	16 15	10 9	4 3 0

operation

source ← SignExtend<sub>64</sub>(Rm);  
REPEAT i FROM 0 FOR 4  
result [i] ← SignExtend<sub>64</sub>(SignExtend<sub>16</sub> (source[i]) );  
Rd ← Register(result [0]);  
Rd+1 ← Register(result [1]);  
Rd+2 ← Register(result [2]);  
Rd+3 ← Register(result [3]);

FIG. 13

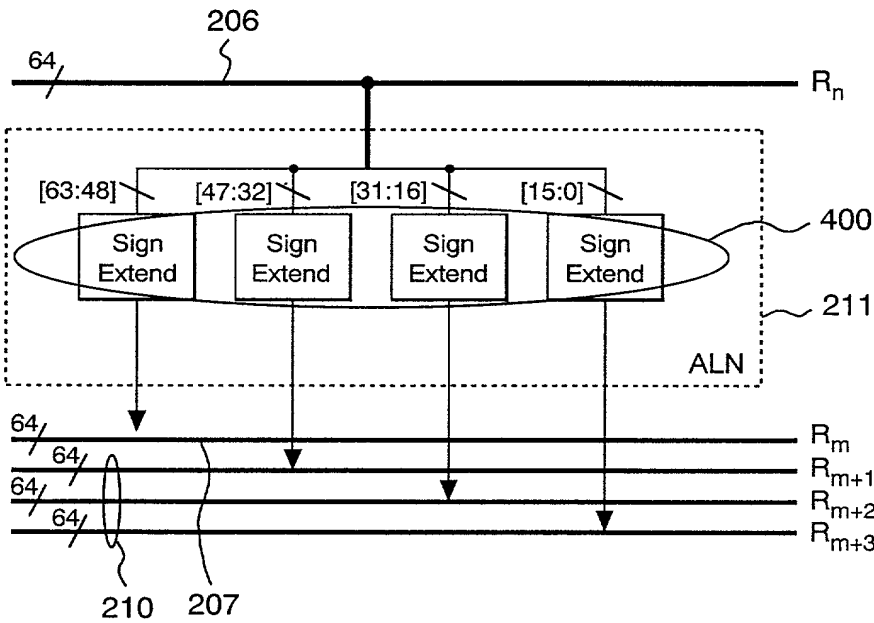
UNPACK.B Rm, Rw, Rd

xxxxxx	m	xxxxx	w	d	0000
31	26 25	20 19	16 15	10 9	4 3 0

operation

source ← SignExtend<sub>64</sub>(Rm);  
REPEAT i FROM 0 FOR 8  
result [i] ← SignExtend<sub>64</sub>(SignExtend<sub>8</sub> (source[i]) );  
Rw ← Register(result [0]);  
Rw+1 ← Register(result [1]);  
Rw+2 ← Register(result [2]);  
Rw+3 ← Register(result [3]);  
Rd ← Register(result [4]);  
Rd+1 ← Register(result [5]);  
Rd+2 ← Register(result [6]);  
Rd+3 ← Register(result [7]);

FIG. 14



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**FIG. 15**

MSHFLE.W Rm, Rn, Rd	xxxxxx	m	xxxxx	n	d	0000
	31 26 25	20 19 16 15	10 9	4 3	0	

operation

```

source1 ← MultiZeroExtend16(Rm);
source2 ← MultiZeroExtend16(Rm+1);
source3 ← MultiZeroExtend16(Rn);
source4 ← MultiZeroExtend16(Rn+1);
REPEAT i FROM 0 FOR 2
{
  result1[i x2] ← source2[i+2]; result1[(i x2)+1] ← source1[i+2];
  result2[i x2] ← source2[i];   result2[(i x2)+1] ← source1[i];
  result3[i x2] ← source4[i+2]; result3[(i x2)+1] ← source3[i+2];
  result4[i x2] ← source4[i];   result4[(i x2)+1] ← source3[i];
}
Rd ← MultiRegister16(result1);
Rd+1 ← MultiRegister16(result2);
Rd+2 ← MultiRegister16(result3);
Rd+3 ← MultiRegister16(result4);

```

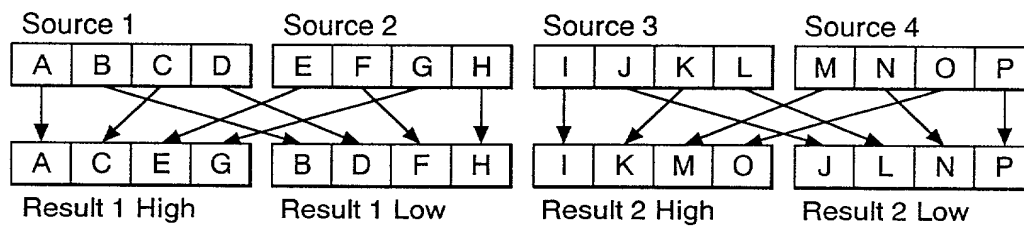
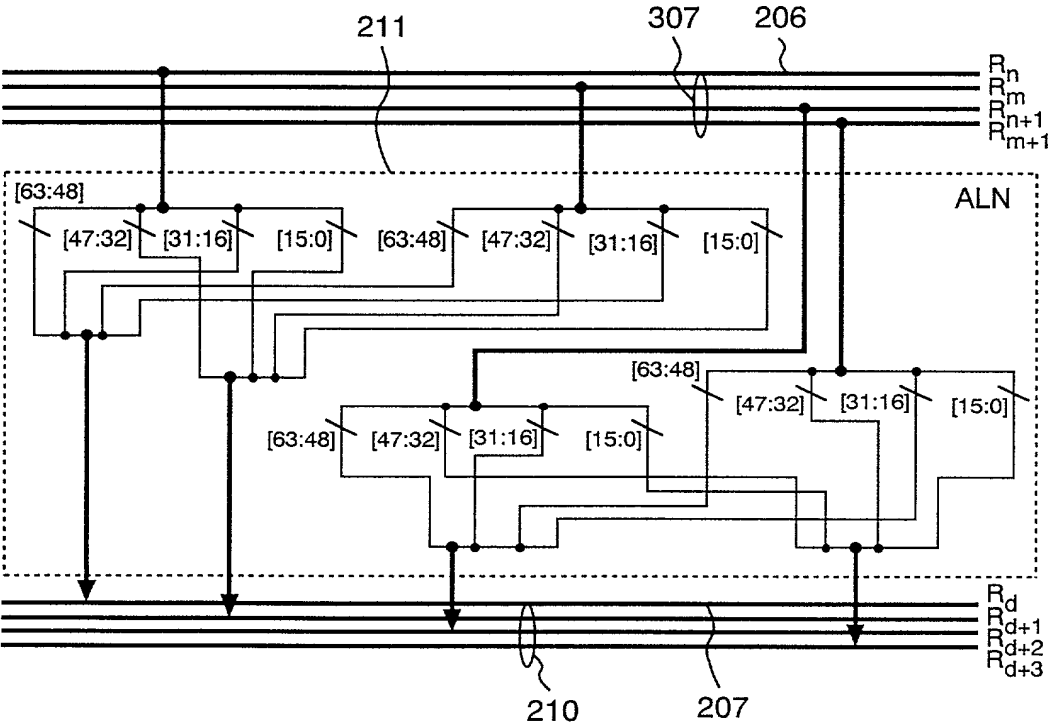
**FIG. 16**

FIG. 17



**FIG. 18**

MSHFHI.W Rm, Rn, Rd

xxxxxx	m	xxxxx	n	d	0000
31 26 25	20 19 16 15	10 9	4 3	0	

operation

```

source1 ← MultiZeroExtend16(Rm);
source2 ← MultiZeroExtend16(Rm+1);
source3 ← MultiZeroExtend16(Rm+2);
source4 ← MultiZeroExtend16(Rm+3);
source5 ← MultiZeroExtend16(Rn);
source6 ← MultiZeroExtend16(Rn+1);
source7 ← MultiZeroExtend16(Rn+2);
source8 ← MultiZeroExtend16(Rn+3);
REPEAT i FROM 0 FOR 2
{
result1[i x2] ← source2[i+2]; result1[(i x2)+1] ← source1[i+2];
result2[i x2] ← source4[i+2]; result2[(i x2)+1] ← source3[i+2];
result3[i x2] ← source6[i+2]; result3[(i x2)+1] ← source5[i+2];
result4[i x2] ← source8[i+2]; result4[(i x2)+1] ← source7[i+2];
}
Rd ← MultiRegister16(result1);
Rd+1 ← MultiRegister16(result2);
Rd+2 ← MultiRegister16(result3);
Rd+3 ← MultiRegister16(result4);

```

**FIG. 19**

MSHFLOW Rm, Rn, Rd

xxxxxx	m	xxxxx	n	d	0000
31 26 25	20 19	16 15	10 9	4 3	0

operation

```

source1 ← MultiZeroExtend16(Rm);
source2 ← MultiZeroExtend16(Rm+1);
source3 ← MultiZeroExtend16(Rm+2);
source4 ← MultiZeroExtend16(Rm+3);
source5 ← MultiZeroExtend16(Rn);
source6 ← MultiZeroExtend16(Rn+1);
source7 ← MultiZeroExtend16(Rn+2);
source8 ← MultiZeroExtend16(Rn+3);
REPEAT i FROM 0 FOR 2
{
result1[i x2] ← source2[i]; result1[(i x2)+1] ← source1[i];
result2[i x2] ← source4[i]; result2[(i x2)+1] ← source3[i];
result3[i x2] ← source6[i]; result3[(i x2)+1] ← source5[i];
result4[i x2] ← source8[i]; result4[(i x2)+1] ← source7[i];
}
Rd ← MultiRegister16(result1);
Rd+1 ← MultiRegister16(result2);
Rd+2 ← MultiRegister16(result3);
Rd+3 ← MultiRegister16(result4);

```

FIG. 20

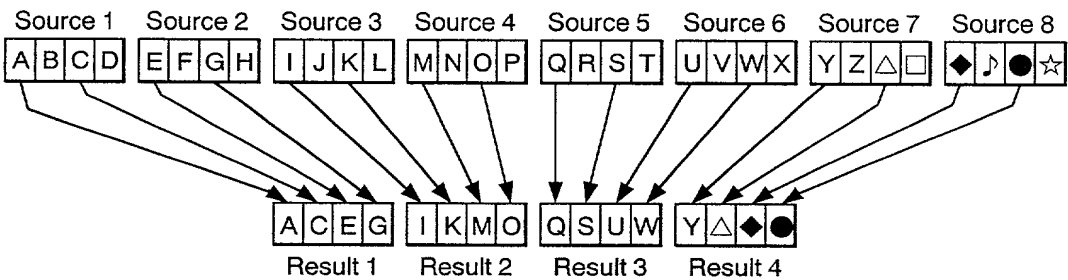
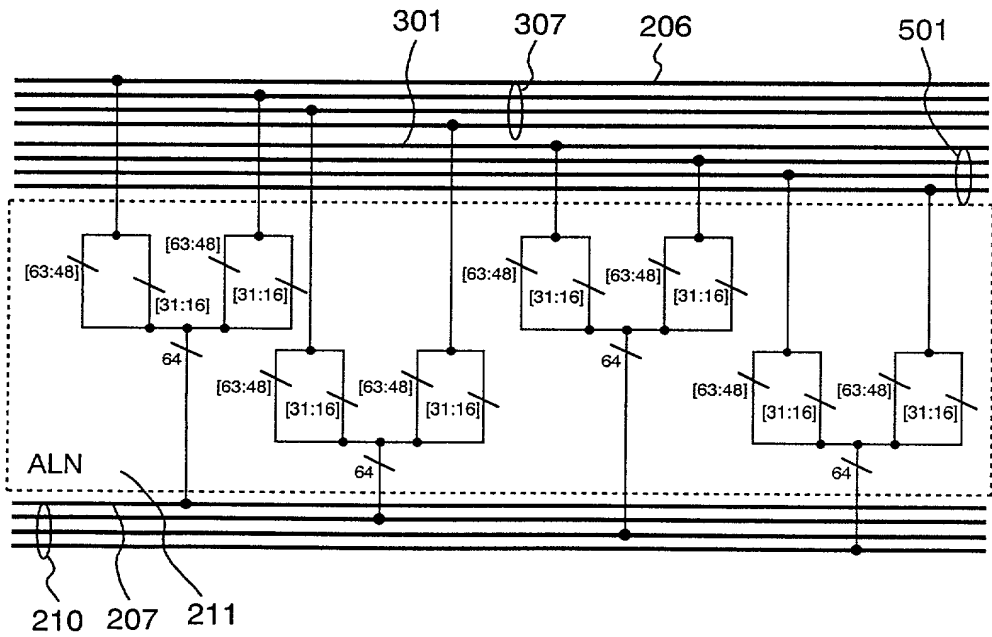
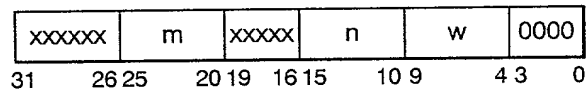


FIG. 21



**FIG. 22**

MMAC.WQ Rm, Rn, Rw



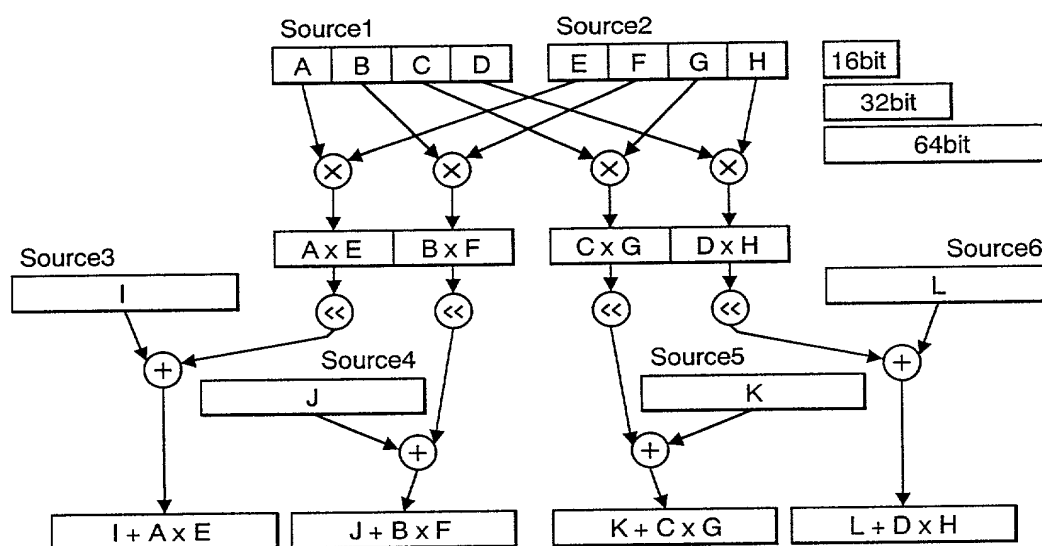
operation

```

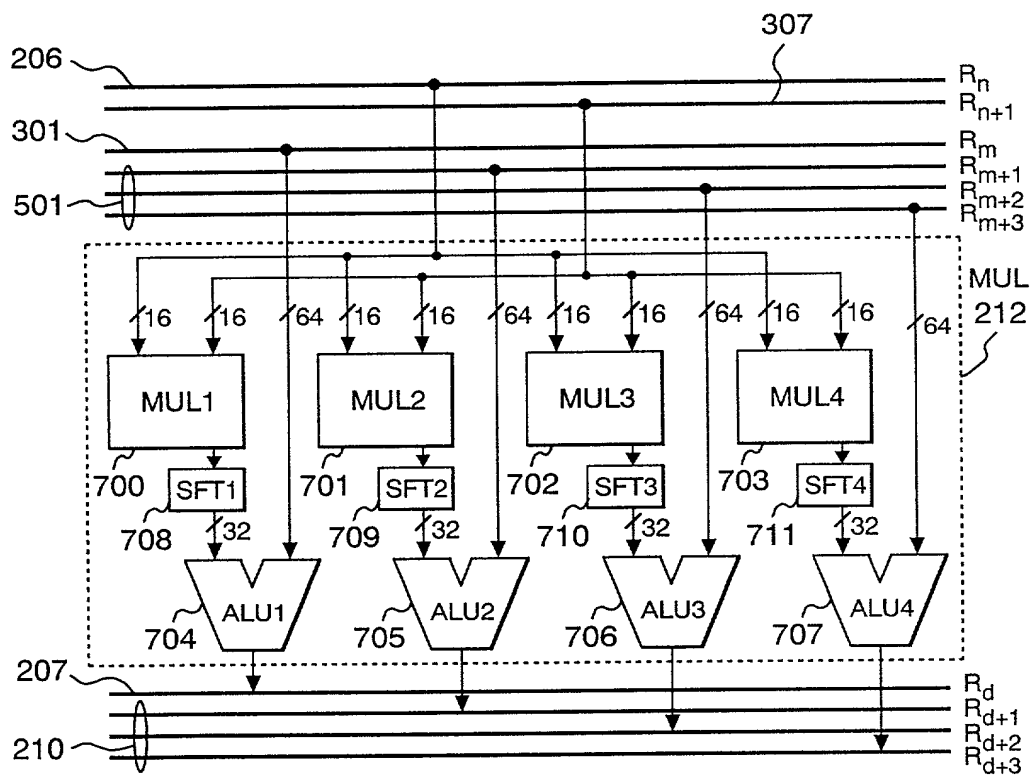
source1 ← MultiSignExtend16(Rm);
source2 ← MultiSignExtend16(Rm+1);
result [0] ← SignExtend64(Rn);
result [1] ← SignExtend64(Rn+1);
result [2] ← SignExtend64(Rn+2);
result [3] ← SignExtend64(Rn+3);
REPEAT i FROM 0 FOR 4
{
temp ← source1[i] x source2[i];
temp ← SignedSaturate64(temp << 1)
result [i] ← SignedSaturate64(result [i] + temp)
}
Rw ← Register(result [0]);
Rw+1 ← Register(result [1]);
Rw+2 ← Register(result [2]);
Rw+3 ← Register(result [3]);

```

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**FIG. 23**

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**FIG. 24**

**FIG. 25A**

mulu.l	r51, r24, r51
mulu.l	r52, r24, r52
mulu.l	r53, r24, r54
mulu.l	r54, r24, r54
shlri	r51, 9, r51
shlri	r52, 9, r52
shlri	r53, 9, r53
shlri	r54, 9, r54
st.w	r17, 0, r51
st.w	r17, 2, r52
st.w	r17, 4, r53
st.w	r17, 6, r54

**FIG. 25B**

mulu.l	r51, r24, r51
mulu.l	r52, r24, r52
mulu.l	r53, r24, r54
mulu.l	r54, r24, r54
pack.w	r51, 9, r55
st.q	r17, 0, r55

**FIG. 26A**

**FIG. 26B**

mshfhi.w	r17, r63, r20	unpack	r17, r17
mshflo.w	r17, r63, r17		
mshfhi.l	r20, r63, r19		
mshflo.l	r20, r63, r20		
mshfhi.l	r17, r63, r21		
mshflo.l	r17, r63, r17		

**FIG. 27A**

**FIG. 27B**

mshfhi.w	r21, r6, r31	mshfle.w	r21, r6, r41
mshflo.w	r21, r6, r21		
mshfhi.w	r31, r21, r41		
mshflo.w	r31, r21, r42		
mshfhi.w	r22, r7, r32		
mshflo.w	r22, r7, r22		
mshfhi.w	r32, r22, r43		
mshflo.w	r32, r22, r44		